530—STGT—IE314

**OPERATION AND
MAINTENANCE MANUAL**

GN Modulator Card

September 2000

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Space Administration

GODDARD SPACE FLIGHT CENTER
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OPERATION AND MAINTENANCE MANUAL

GN MODULATOR CARD

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DCN CONTROL SHEET

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1−1   Introduction

1−1.1 The Ground Network (GN) Modulator (GMOD) Printed Wire Assembly (PWA) is designed to be installed in the NASA Second TDRSS Ground Terminal (STGT) Modulator/Doppler Predictor (MDP).

1−1.2 The GMOD PWA performs the following phase modulation.

a. Sinewave Subcarrier: PCM coded data is used to BPSK-modulate a sinusoidal subcarrier, which is used to phase modulate the carrier at varying modulation indices (PCM/PSK/PM).

b. Direct Carrier: PCM coded data used to directly phase modulates the carrier at varying modulation indices (PCM/PM).

c. Squarewave Subcarrier: PCM coded data is used to modulate a squarewave subcarrier (exclusive-OR operation), which is used to phase modulate the carrier at varying modulation indices.

1−1.3 These modulation formats are compatible with the command signal formats of many Low Earth Orbiting (LEO) satellites that utilize direct earth-to-space command and telemetry communication links. Modulation indices used with these modulation formats are nearly always such that a residual carrier is present. (A residual carrier allows for the use of a simple phase-lock-loop to provide transponder carrier tracking.) NASA has traditionally supported this class of satellites via the NASA Ground Network (GN).

1−1.4 The NASA Space Network (SN) supports LEO satellites via the NASA Tracking, Data, and Relay Satellite System (TDRSS), thus utilizing an earth-to-space-to-space relay for command and telemetry communications. Satellites that have traditionally utilized the SN for command and telemetry have used suppressed carrier modulation formats (BPSK and QPSK), per the original NASA SN specification.

1−1.5 The GMOD card has been manufactured for use in the NASA Space Network (SN) to support satellites traditionally supported via the GN. For this reason, this card has been named the GN Modulator card, differentiating its modulation formats from those traditionally supported via the SN. Likewise, the modulation formats it supports are frequently identified herein, as well as within the parts of the NASA SN community, as GN modulation formats.

1−2   Functional Summary

The following functions are provided by the GMOD PWA:

a. Control/Status communication between the GMOD PWA and the VMEbus.

b. PCM data format conversion of received NRZ-L data.

c. "Elastic" buffering of input data to accommodate an asynchronous relationship between the input data and modulation data clock.

d. Sinewave subcarrier modulation of a carrier by a BPSK-modulated subcarrier (PCM/PSK/PM).

e. Squarewave subcarrier modulation of a carrier by a BPSK-modulated squarewave.

f. Direct modulation of carrier by PCM formatted data (PCM/PM).

g. The capability to modulate the carrier (or subcarrier) with an idle pattern consisting of alternating 1's and 0's when the input clock signal is static.

1−3   Applicable Documentation

Table 1−1 provides a list of GMOD applicable documents.

Table 1—1. Applicable Documents	
WSC Controlled Documents	
Document/Drawing Number	Title
WSC—1547558	GN Modulator Printed Wiring Assembly
WSC—1547559	GN Modulator Card Schematic/Logic Diagram
WSC—1547560	GN Modulator, Data Conditioner FPGA Schematic/Logic Diagram
WSC—1547561	GN Modulator, Modulator FPGA Schematic/Logic Diagram
530-STGT-IE310	Operations and Maintenance Manual, Modulator/Doppler Predictor
530-STGT-IE314/Supplement	GN Modulator Card Vendor Data Sheets, Supplement to 530-STGT-IE314
Standards	
Document/Drawing Number	Title
IEEE 1014	VME Bus Specification
Vendor Documents	
Vendor	Title
Atmel	ATDH2200E Programming Kit User Guide

Section 2 — Requirements

2−1 Carrier Modulation

2−1.1 Direct Data Modulation

The carrier can be modulated directly by the optionally formatted command data. Input command data will phase shift modulate the IF carrier. The signal will be parameterized by the user configurations listed in Table 2−1.

2−1.2 Subcarrier Modulation

The input command data can be used to BPSK modulate a sinusoidal or square-wave subcarrier, which in turn will be used to linearly phase modulate the carrier. Data transitions will be coherent with the subcarrier zero crossings. The ratio (R) of the subcarrier frequency divided by the data rate can be 2, 4, 8, 16, 32, 64, or 128. (The subcarrier frequency must be a power-of-two multiple of the data rate.) The data rate is further constrained by the minimum and maximum data rates of 125 bps and 8,000 bps, respectively. For example, if a 16 kHz subcarrier is specified, the valid data rates for NRZ formats would be 8,000, 4,000, 2,000, 1,000, 500, 250, and 125 bps, corresponding to the values of R equal to 2, 4, 8, 16, 32, 64, and 128, respectively.

The signal will be parameterized by the user configurations listed in Table 2−2.

Table 2−1. Direct Data Modulation Parameters		
Modulation Parameter	Accepted Values	Precision
Modulation Index	0.2 to 1.5 radians, or BPSK (π/2 radians)	0.1 radian
Data Rate	125 bps to 1Mbps, NRZ, or 125 bps to 500 kbps, Bi-phase	1 bps
PCM Waveforms	NRZ-L, NRZ-M, NRZ-S, Bi-phase-L, Bi-phase-M, Bi-phase-S	N/A

Table 2−2. Subcarrier Modulation Parameters		
Modulation Parameter	Accepted Values	Precision
Subcarrier Frequency	2 kHz − 16 kHz	1 Hz
Subcarrier Type	Square Wave or Sinusoidal	N/A
Modulation Index	0.2 to 1.8 radians	0.1 radian
Subcarrier to Data Rate Ratio (R)	2,4,8,16,32,64,128, NRZ, or 4,8,16,32,64,128, Bi−phase (with min/max constraint of 125 bps to 8 kbps)	N/A
PCM Waveforms (applied to subcarrier modulation)	NRZ-L, NRZ-M, NRZ-S, Bi-phase-L, Bi-phase-M, Bi-phase-S	N/A

2−2   Idle Pattern Generation

The GMOD PWA will provide the following idle pattern capability for all data rates less than or equal to 8000 bps. The GMOD will optionally modulate the carrier or subcarrier with an idle pattern when there is no user command clock present. The idle pattern will be repeating data bits of "10", regardless of data format selected. There will be no control of "last idle bit" prior to command data modulation or "first idle bit" following command data modulation. When this option is selected, the idle pattern will modulate the subcarrier (or carrier) at all times that data modulation is enabled and command data is not present. For data rates greater than 8000 bps, no idle pattern capability will be provided.

2−3   Performance Requirements

Table 2−3 provides performance requirements not otherwise provided above.

Table 2−3. Additional Performance Requirements	
Performance Parameter	Requirement
Subcarrier Frequency Accuracy	± 0.5 Hz
Data transition and subcarrier coherency	transitions occur at subcarrier zero crossing within $\pm$ 1 degree
Modulation index accuracy	$\pm$ 10%

Section 3 — Functional Description

3−1 General

The GMOD card is a digital phase modulator. It is implemented on a standard A24:D16 VMEbus card. It generates a modulated IF waveform by Direct Digital Synthesis (DDS) techniques; that is, the signal is synthesized as a digital representation of the desired waveform, and is then converted to an analog signal by a Digital to Analog Converter (DAC).

Refer to Figure 3−1 for the functional block diagram of the GN Modulator Card.

3−2 Baseband Processing

The GMOD card receives baseband data and clock signals. Various baseband processing functions are required prior to this data being applied to the IF waveform generation. Most baseband processing is performed by the Data FPGA.

3−2.1 FIFO Data Buffering

For some configurations, baseband data processing must be performed synchronously to a local clock generated by the GMOD PWA. The input Data and Clock signals presented to the GMOD card are typically asynchronous to this clock; there may also be a finite frequency difference between the external clock and the GMOD clock. For this reason, an "elastic data buffer" is required. This function is provided by a First-in-First-Out (FIFO) memory IC.

3−2.2 Idle Pattern Generation

The GMOD can optionally generate an idle pattern to be applied to the modulated signal in the absence of user data. If enabled, a repeating "10" idle pattern will be generated when the input clock signal is idle. This Idle pattern will be presented to the data format circuit. Because there cannot be a phase discontinuity between the user data stream and the idle pattern, the FIFO Data Buffering must be utilized when Idle Pattern Generation is enabled.

3−2.3 Data Format Conversion

The GMOD card receives NRZ-L data and optionally formats the data to any one of the following data formats: NRZ-M, NRZ-S, biphase-L, biphase-M, or biphase-S. This data format conversion will also be performed on the idle pattern when enabled.

3−2.4 Clock Divide

For subcarrier modes, the data rate is restricted to values such that the ratio of the subcarrier frequency to the data rate is a power of two. For example, for a subcarrier frequency of 16,000 Hz, allowable data rates would be 8,000 bps, 4,000 bps, 2,000 bps, etc. Also in the case of subcarrier modes, the data transitions must be coincident with the subcarrier zero-crossings. Because of these constraints in the signal design, the data clock must be derived from the subcarrier waveform. The data processing FPGA is provided a subcarrier clock (the most significant bit of the digital subcarrier that is generated by the Modulator FPGA). A clock divide circuit is utilized to derive a data clock that is coherent with the subcarrier.

3−3 Phase Modulator

The DDS modulator synthesizes an 8.5 MHz digital carrier. The digital processing of this synthesis is performed by the Modulator FPGA. The 8.5 MHz carrier can be modulated by three different modulation formats.

3−3.1 Direct Phase Modulation

The carrier can be phase modulated directly by the PCM waveform. Modulation indices from 0.2 to 1.5 radians, in 0.1 radian increments, are supported in this mode. BPSK modulation is also supported.

3−3.2 Subcarrier Modulation

The DDS modulator generates a digital sinewave subcarrier. The subcarrier frequency is controlled
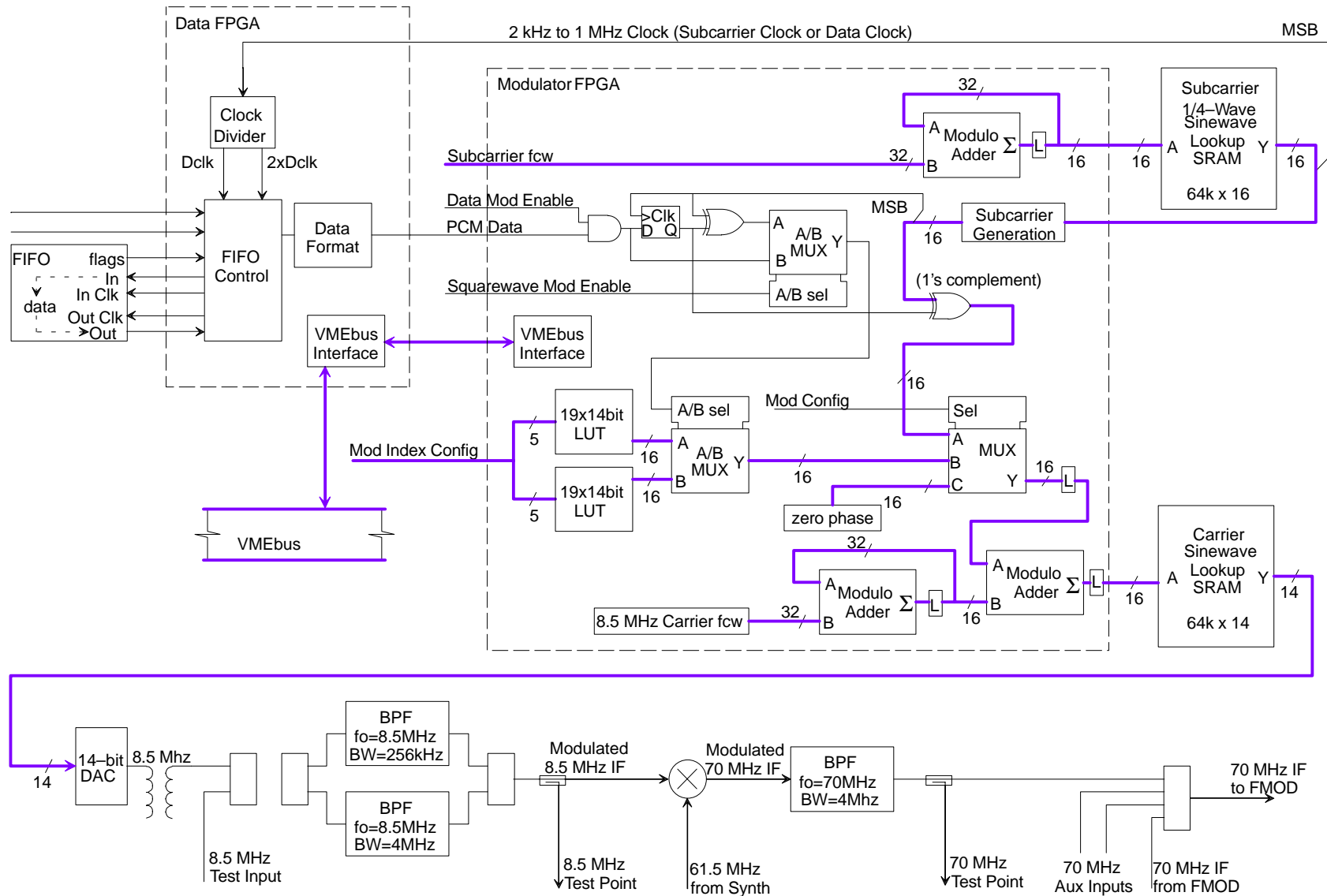
Figure 3—1. GN Modulator Card Functional Block Diagram

via the VMEbus interface. This subcarrier can be BPSK modulated (digitally) by the PCM waveform, and the carrier can then be PM-modulated (digitally) by the modulated subcarrier. Modulation indices from 0.2 to 1.8 radians, in 0.1 radian increments, are supported in this mode.

Alternatively, the most significant bit of the sine-wave subcarrier (which represents a squarewave subcarrier of the same frequency) can be BPSK-modulated (digitally) by the PCM waveform; this modulated squarewave subcarrier can then be used to phase modulate (digitally) the carrier. Modulation indices from 0.2 to 1.5 radians, in 0.1 radian increments, are supported in this mode. A modulation index of $\pi/2$ radians is also supported (suppressed carrier).

For subcarrier modulation, all data transitions must be coincident with subcarrier zero crossings.

3−4 Analog to Digital Conversion

The digital 8.5 MHz IF output of the DDS modulator is presented to a 14-bit Digital-to-Analog Convert-er (DAC), which generates an 8.5 MHz analog IF signal.

3−5 IF Processing

The analog 8.5 MHz IF DAC output signal is filtered by either a 256 kHz bandpass filter or a 4 MHz bandpass filter. This filtered 8.5 MHz IF signal is upconverted to 70 MHz by a 61.5 MHz LO received from an external source. This 70 MHz IF is presented to a four-to-one switch, which selects one of four IF signals to be presented to the GMOD 70 MHz IF output. The other three 70 MHz IF signals presented to the IF switch are received from external source.

3−6 VMEbus Interface

The GMOD is an A24:D16, slave VMEbus card, conforming to the IEEE 1014 VMEbus specification. In the MDP, the GMOD card is controlled by the MCP card via the MDP VMEbus.

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Section 4 — Physical Description

4−1   Physical Characteristics

The following describes the physical characteristics of the GN Modulator:

a.   6-layer printed circuit board (PCB)

b.   VME double-height (9.2" x 6.3")

c.   Dual 96-pin backplane connectors (DIN 41612)

d.   One front panel mounted 50-pin connector

e.   Eight front panel mounted SMB coaxial connectors

4−2   PCB Description

The GMOD PCB and its front panel are illustrated in Figure 4−1. Most of the GMOD digital processing is implemented in two Xilinx Spartan-II FPGAs. The Data Conditioning FPGA processes incoming data and generates a PCM waveform to be used to modulate the carrier or subcarrier. The Modulation FPGA synthesizes a digital representation of an 8.5 MHz, modulated IF signal, using the PCM waveform to modulate the carrier (or subcarrier). This digital waveform is converted to an analog IF signal by the Digital to Analog Converter (DAC). The 8.5 MHz signal is bandpass filtered, upconverted to 70 MHz. This 70 MHz IF signal is the primary output of the GMOD PCB.

The signal flow through the various physical devices of the GMOD is illustrated in Figure 4−2.

4−3   Interface Definition

Refer to Figure 4−3 for location of connectors and jumper fields.

4−3.1   P1 and P2 Connectors

All pins of the P1 connector and many pins of the P2 connector are part of the VMEbus interface; refer to the VMEbus specification for descriptions of these signals.

Reference Table 4−1 for the P1 connector interface definitions and Table 4−2 for the P2 connector interface definitions.

4−3.2   P3 Connector (Test Signals)

Reference Table 4−3 for the P3 connector interface definitions.

4−3.3   RF Connectors

Reference Table 4−4 for the RF connector interface definitions.

4−3.4   JP2 and JP3, FPGA EEPROM In-Circuit Programming Ports

JP2 and JP3 provide an in-circuit programming capability for the Atmel configuration EEPROMs that contain the Data FPGA configurations, respectively. The pin-outs of JP2 and JP3 are identical, and conform to the interface required for the Atmel ATDH2200E, "FPGA Configurator Programming Kit."

Reference Table 4−5 for JP2 and JP3 interface definitions.
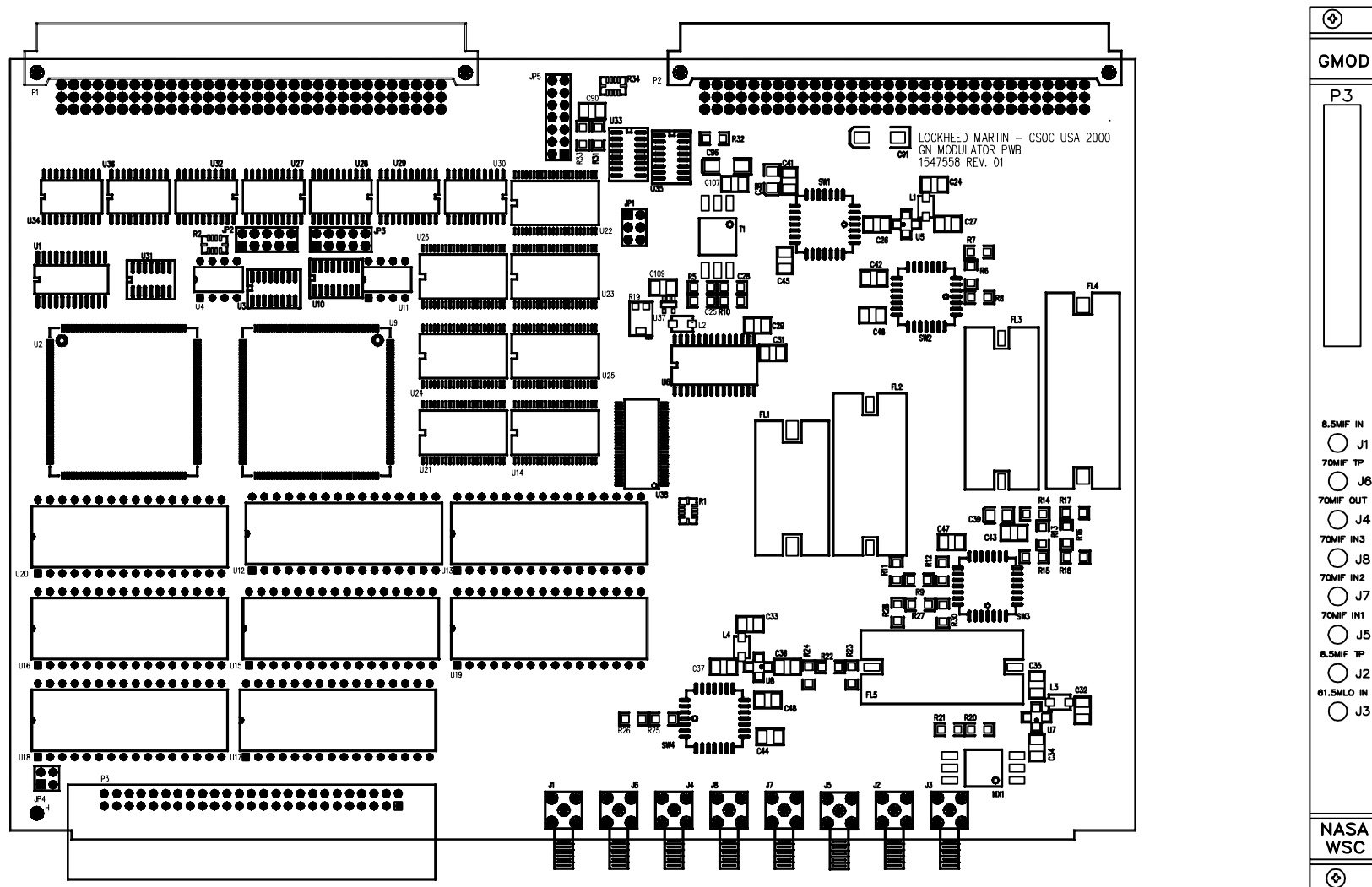
00015.DWG

Figure 4−1. GN Modulator PCB and Front Panel
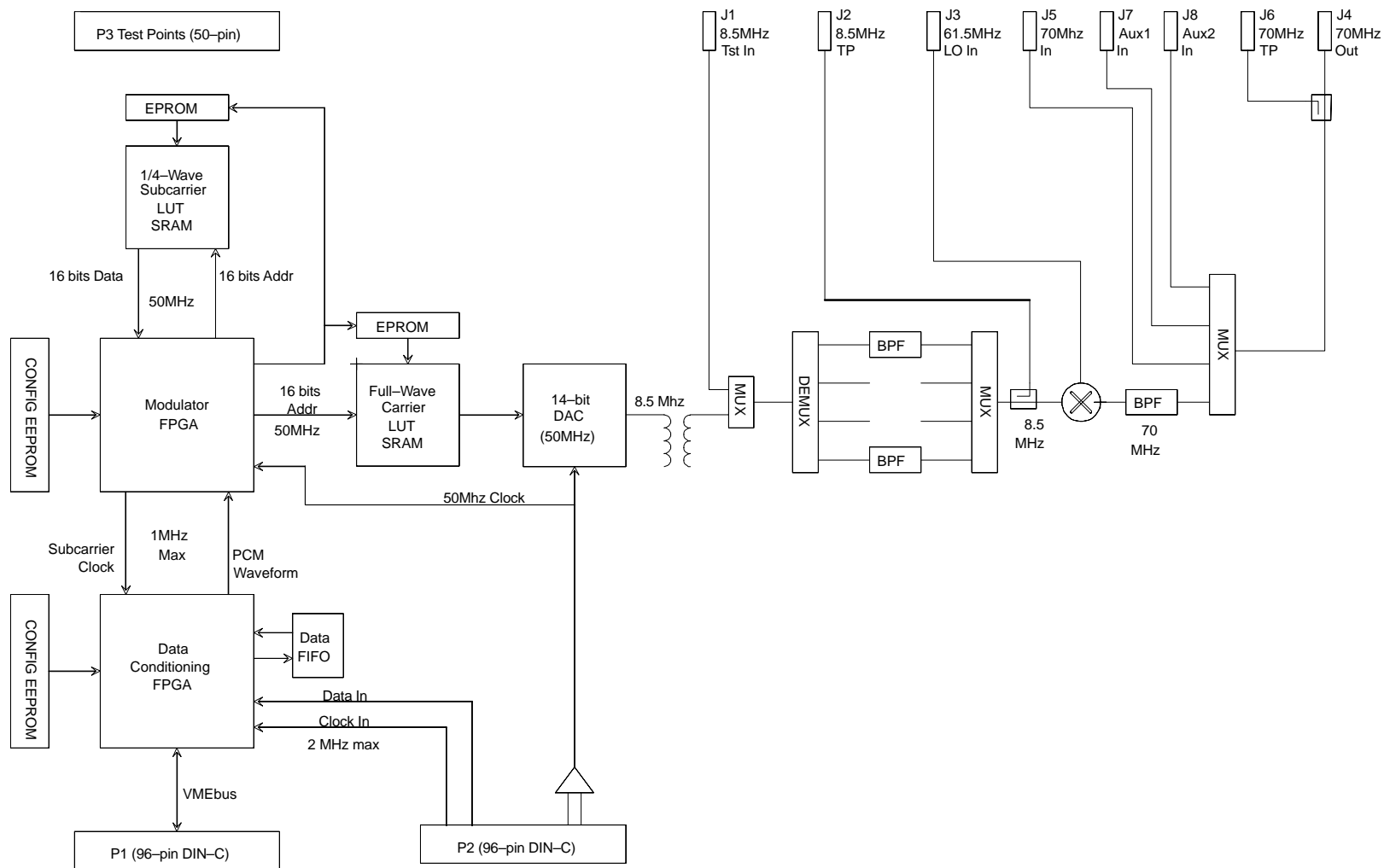
Figure 4—2. GMOD Signal Flow Block Diagram

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JP5

P2

P1

LOCKHEED MARTIN — CSOC USA 2000
GN MODULATOR PWB
1547558 REV. 01

JP1

JP2 JP3

R19

JP4

P3

J1 J6 J4 J8 J7 J5 J2 J3
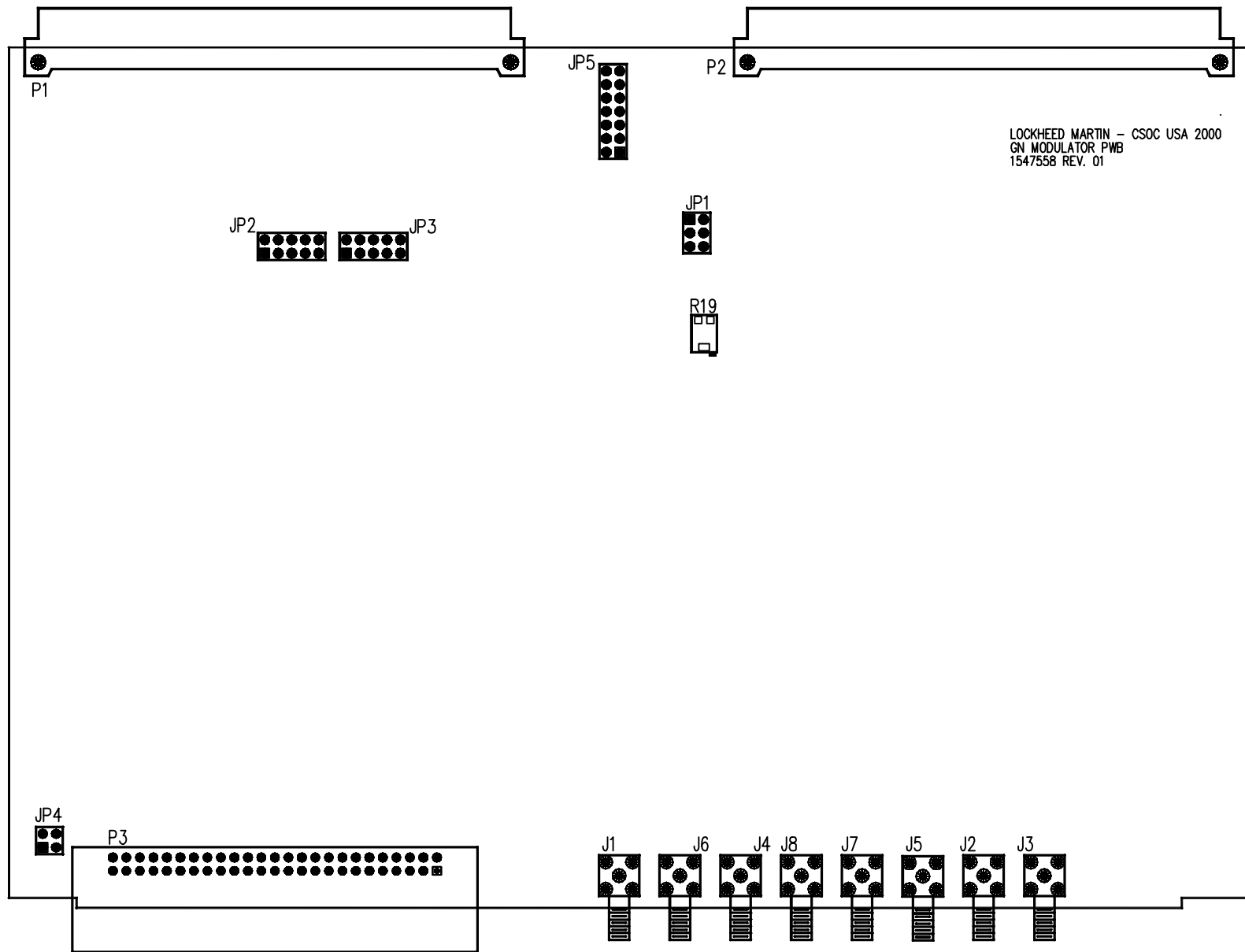
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Figure 4—3. GMOD PCB Connectors and Jumper Fields

Table 4−1. P1 Connector Interface		
Pin No.	**Signal Name**	**Description**
A1	D0	VMEbus Signal
B1	−	
C1	D8	VMEbus Signal
A2	D1	VMEbus Signal
B2	−	
C2	D9	VMEbus Signal
A3	D2	VMEbus Signal
B3	−	
C3	D10	VMEbus Signal
A4	D3	VMEbus Signal
B4	BG0 In	VMEbus Signal
C4	D11	VMEbus Signal
A5	D4	VMEbus Signal
B5	BG0 Out	VMEbus Signal
C5	D12	VMEbus Signal
A6	D5	VMEbus Signal
B6	BG1 In	VMEbus Signal
C6	D13	VMEbus Signal
A7	D6	VMEbus Signal
B7	BG1 Out	VMEbus Signal
C7	D14	VMEbus Signal
A8	D15	VMEbus Signal
B8	BG2 In	VMEbus Signal
C8	D15	VMEbus Signal
A9	GND	Digital Ground
B9	BG2 Out	VMEbus Signal
C9	GND	Digital Ground
A10	VmeClk	VMEbus Signal
B10	BG3 In	VMEbus Signal
C10	−	
A11	GND	Digital Ground
B11	BG3 Out	VMEbus Signal
C11	−	
A12	DS1_Neg	VMEbus Signal

Note: "−" indicates no connection

Pin No.	Signal Name	Description
**Table 4−1. P1 Connector Interface (Continued)**
Pin No.	Signal Name	Description
B12	−	
C12	SYSRST_Neg	VMEbus Signal
A13	DS0_Neg	VMEbus Signal
B13	−	
C13	LWORD_Neg	VMEbus Signal
A14	WRT_Neg	VMEbus Signal
B14	−	
C14	AM5	VMEbus Signal
A15	GND	Digital Ground
B15	−	
C15	A23	VMEbus Signal
A16	DTACK_Neg	VMEbus Signal
B16	AM0	VMEbus Signal
C16	A22	VMEbus Signal
A17	GND	Digital Ground
B17	AM1	VMEbus Signal
C17	A21	VMEbus Signal
A18	AS_Neg	VMEbus Signal
B18	−	
C18	A20	VMEbus Signal
A19	GND	Digital Ground
B19	AM3	VMEbus Signal
C19	A19	VMEbus Signal
A20	IACK_Neg	VMEbus Signal
B20	GND	Digital Ground
C20	A18	VMEbus Signal
A21	IACKIN_Neg	VMEbus Signal
B21	−	
C21	A17	VMEbus Signal
A22	IACKOUT_Neg	VMEbus Signal
B22	−	
C22	A16	VMEbus Signal
A23	AM4	VMEbus Signal
B23	GND	Digital Ground
C23	A15	VMEbus Signal

Note: "−" indicates no connection

Pin No.	Signal Name	Description
	Table 4−1. P1 Connector Interface (Continued)	
A24	A7	VMEbus Signal
B24	IRQ7_Neg	VMEbus Signal
C24	A14	VMEbus Signal
A25	A6	VMEbus Signal
B25	IRQ6_Neg	VMEbus Signal
C25	A13	VMEbus Signal
A26	A5	VMEbus Signal
B26	IRQ5_Neg	VMEbus Signal
C26	A12	VMEbus Signal
A27	A4	VMEbus Signal
B27	IRQ4_Neg	VMEbus Signal
C27	A11	VMEbus Signal
A28	A3	VMEbus Signal
B28	IRQ3_Neg	VMEbus Signal
C28	A10	VMEbus Signal
A29	A2	VMEbus Signal
B29	IRQ2_Neg	VMEbus Signal
C29	A9	VMEbus Signal
A30	A1	VMEbus Signal
B30	IRQ1_Neg	VMEbus Signal
C30	A8	VMEbus Signal
A31	−	
B31	VCC	Digital+5V Supply
C31	−	
A32	VCC	Digital+5V Supply
B32	VCC	Digital+5V Supply
C32	VCC	Digital+5V Supply

Note: "−" indicates no connection

Table 4−2. P2 Connector Interface		
Pin No.	**Signal Name**	**Description**
A1	GND_AN	Analog Ground
B1	VCC_AN	Analog +5V Supply
C1	–	
A2	GND_AN	Analog Ground
B2	GND_AN	Analog Ground
C2	GND_AN	Analog Ground
A3	VEE	Analog −5V Supply
B3	VEE	Analog −5V Supply
C3	VEE	Analog −5V Supply
A4	–	
B4	BAS23	Address-23, configures GMOD for Address Range Assigned to slot
C4	ECL50MHZ_P	50 MHz Clock, Differential ECL
A5	–	
B5	BAS22	Address-22, configures GMOD for Address Range assigned to slot
C5	ECL50MHZ_N	50 MHz Clock, Differential ECL
A6	–	
B6	BAS21	Address-21, configures GMOD for Address Range assigned to slot
C6	–	
A7	–	
B7	BAS20	Address-20, configures GMOD for Address Range assigned to slot
C7	–	
A8	–	
B8	BAS19	Address-19, configures GMOD for Address Range assigned to slot
C8	–	
A9	–	
B9	–	
C9	–	
A10	COMDATA_P	Data In, Differential ECL
B10	–	
C10	–	
A11	COMDATA_N	Data In, Differential ECL
B11	–	
C11	–	
A12	COMCLK_P	Data Clock In, Differential ECL

Note: "−" indicates no connection

Table 4−2. P2 Connector Interface (Continued)

Pin No.	Signal Name	Description
B12	GND_AN	Analog Ground
C12	−	
A13	COMCLK_N	Data Clock In, Differential ECL
B13	VCC_AN	Analog +5V Supply
C13	−	
A14	GND_AN	Analog Ground
B14−A22	−	
B22	GND_AN	Analog Ground
C22−A31	−	
B31	GND_AN	Analog Ground
C31	−	
A32	−	
B32	VCC_AN	Analog +5V Supply
C32	−	

Note: "−" indicates no connection

Pin No.	Signal Name	Description
1	ExtDataIn	Data In, TTL
2	ExtClkIn	Data Clock In, TTL
3	No_Clk_In	No Clock Present Flag
4	NRZL_to_Formatter	NRZ-L Data, prior to data format conversion (post-FIFO)
5	Clock_to_Formatter	Data Clock that drives data format conversion process
6	2X_Clock	2-Times data clock (post-FIFO)
7	SubcarClk	Subcarrier Clock
8	DivClk	Output of Clock divide circuit
9	PCM_Data	Formatted Data (post-data format conversion process)
10	Clock	Clock for PCM Data
11	Clock_Neg	Inverted Clock for PCM Data
12	Fifo_Empty	FIFO Empty Flag
13	Fifo_Half_Full	FIFO Half Full Flag
14	FifoWrtClk	FIFO Write Clock (FIFO input)
15	FifoRdClk	FIFO Read Clock (FIFO output)
16	EdgePulse	Input Clock Rising Edge pulses
17	PRE	Ran AND ReadEna
18	Fifo_Mty_Error	Status bit indicating the FIFO underrun has occurred
19	Fifo_Full_Error	Status bit indicating the FIFO overrun has occurred
20	Fifo_Reset_Neg	Copy of FIFO Reset signal, driven by Data FPGA
21	SubCar_Test_Input	For use with external subcarrier "test" clock
22	INIT_Neg	Xilinx FPGA control signal, ganged to both Mod and Data FPGAs
23	PROG_Neg	Xilinx FPGA control signal, ganged to both Mod and Data FPGAs
24	TDO	Data Output of FPGA JTAG chain
25	VCC	Digital +5V Supply
26	TTL50MHZ−B	50 MHz Clock, TTL
27	Mod_TP0	Modulator Test Point, Bit−0 of switched internal databus sample
28	Mod_TP1	Modulator Test Point, Bit−1 of switched internal databus sample
29	Mod_TP2	Modulator Test Point, Bit−2 of switched internal databus sample
30	Mod_TP3	Modulator Test Point, Bit−3 of switched internal databus sample
31	Mod_TP4	Modulator Test Point, Bit−4 of switched internal databus sample
32	Mod_TP5	Modulator Test Point, Bit−5 of switched internal databus sample
33	Mod_TP6	Modulator Test Point, Bit−6 of switched internal databus sample
34	Mod_TP7	Modulator Test Point, Bit−7 of switched internal databus sample
35	Mod_TP8	Modulator Test Point, Bit−8 of switched internal databus sample

Table 4−3. P3 Connector Interface

Pin No.	Signal Name	Description
		Table 4−3. P3 Connector Interface (Continued)
36	Mod_TP9	Modulator Test Point, Bit−9 of switched internal databus sample
37	Mod_TP10	Modulator Test Point, Bit−10 of switched internal databus sample
38	Mod_TP11	Modulator Test Point, Bit−11 of switched internal databus sample
39	Mod_TP12	Modulator Test Point, Bit−12 of switched internal databus sample
40	Mod_TP13	Modulator Test Point, Bit−13 of switched internal databus sample
41	Mod_TP14	Modulator Test Point, Bit−14 of switched internal databus sample
42	Mod_TP15	Modulator Test Point, Bit−15 of switched internal databus sample
43	Mod_TP16	Modulator Test Point 16
44	Mod_TP17	Modulator Test Point 17
45	Mod_TP18	Modulator Test Point 18
46	Mod_TP19	Modulator Test Point 19
47	TCK	JTAG Chain Clock
48	TMS	JTAG Chain Control Signal
49	TDI	Data Output of FPGA JTAG chain
50	GND	Digital Ground

Table 4−4. RF Connectors, Interface		
Pin No.	**Signal Name**	**Description**
J1	SL2	8.5 MHz IF Test Input
J2	SL18	8.5 MHz IF Test Point, post-Bandpass filter
J3	SL29	61.5 MHz LO Input
J4	SL27	70 MHz IF Output
J5	SL24	70 MHz IF Input No. 1
J6	SL28	70 MHz IF Test Point
J7	SL25	70 MHz IF Input No. 2
J8	SL26	70 MHz IF Input No. 3

Table 4−5. JP2 and JP3, FPGA Configuration EEPROM In-Circuit Programming Ports		
Pin No.	**Signal Name**	**Description**
1	D_DIN	Serial programming Data
2	D_XDONE	Programming Done Flag
3	D_XSCLK	Programming Clock
4	D_XINT_N	Programming Initialization
5	−	
6	−	
7	GND	Digital Ground
8	VCC	Digital +5V Supply
9	−	
10	D_SER_EN	Enable In-circuit programming (switch multiplexer)

Note: "−" indicates no connection

Section 5 — Operation

The GMOD PWA is controlled via the VMEbus interface. Appendix A and Appendix B provide tables of the GMOD VMEbus addresses map; refer to these tables for the following discussion.

Most of the GMOD write-registers are configuration registers; they configure the GMOD logic and the IF switches. It is via these configuration registers that the hardware is configured and the parameters set for the desired data and modulation formats.

Several GMOD registers are better described as control registers; they initiate some action or enable some function of the GMOD card. These registers include the reset registers, the Data Control Run bit, the SRAM Load Register, and the Modulator Run register.

Operation of the GMOD card involves three general steps: 1) Initialization of all configuration registers; 2) Loading the SRAM (if this has not been done since a power cycle); and 3) Manipulating the control registers to enable necessary processing. The first two steps can be performed in any order, but both must be performed prior to

enabling the modulator functions. The SRAM load function should only be required after a power-off condition. This manual will not provide a detailed operational example; however, the following guidelines should be followed.

After a power cycle and prior to enabling the Modulator FPGA, the SRAM Load must be performed.

If the FIFO is to be enabled for a configuration, it should be enabled after all FIFO configuration registers have been initialized. A FIFO reset should always be implemented immediately following the FIFO enable bit being set.

The FIFO should be enabled whenever Idle Pattern is enabled. The FIFO should be enabled for all Subcarrier Modulation configurations, regardless of Idle Pattern configuration.

With the exception of the SRAM Load and FIFO configurations, all configuration parameters can be changed "on the fly" (while the modulator is running).

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Section 6 — Maintenance

6−1 Adjustment Procedures

There are no adjustment or alignment procedures that must be performed on a periodic basis for the GMOD PWA.

There is one adjustable component on the GMOD card. R19 is a potentiometer that provides an adjustment of the DAC full-scale output voltage. R19 is set to 2,000 Ohms upon receipt of the board from the PCB manufacturer and should remain at this value. (See Figure 4−3 for the location of R19).

6−2 Jumper Fields

6−2.1 JP1, FIFO Configuration Override

The TI 74ACT2228 FIFO IC is a dual FIFO integrated circuit. The FIFO to be used is configured via the VMEbus interface by the firmware. Jumper Field 1 allows for overriding the firmware selection. Installing Jumper−3 (between pins five and six) causes the Data_FPGA to select the FIFO circuit dictated by the presence or absence of other jumpers of JP1. If Jumper−3 is not installed, jumpers in positions one and two have no effect.

If Jumper−3 is installed, and Jumper−1 and Jumper−2 are not installed, the Data FPGA will route all data through FIFO−1, regardless of the contents of the FIFO control register. If Jumper−3 is installed, and Jumper−1 and Jumper−2 are both installed, the Data FPGA will route all data through FIFO−2, regardless of the contents of the FIFO control register. Under no circumstances should Jumper−1 and Jumper−2 be configured differently.
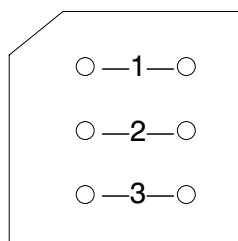

Figure 6−1. JP1

6−2.2 JP4, FPGA Programming Configuration

JP4 determines what signal drives the Program Pins for both the Data FPGA and the Modulator FPGA. If no jumpers are installed on JP4, both FPGAs will be programmed only at power-on. If Jumper−1 is installed, a VMEbus reset will cause the FPGAs to be reprogrammed. If Jumper−2 is installed, the PROG_Neg signal (Pin−23 of the P3 Test Connector) will drive the FPGA program signal. Under this configuration, FPGA reprogramming could be forced by grounding Pin−23 of the P3 Test Connector.
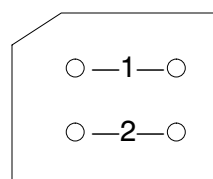

Figure 6−2. JP4

6−2.3 JP5, IRQ Configuration (Reserved for Future Use)

The GMOD card does not generate VMEbus interrupts. However, the design includes the circuitry necessary to add interrupt-processing logic to the Data FPGA. JP5 selects the VMEbus interrupt level the GMOD interrupt would generate if this feature were included in the data FPGA. If this feature is implemented, only one jumper should be installed on JP5. The position of the jumper on the jumper field would correspond to the VMEbus interrupt level (one through seven). Jumpers should not be installed on Jumper field 5 (JP5) for the current version of the Data FPGA.
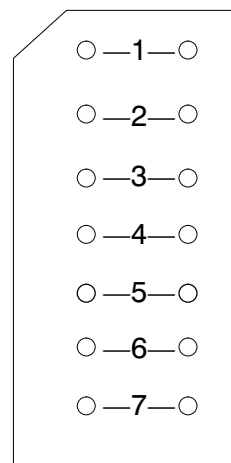

Figure 6−3. JP5

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Section 7 — Theory of Operation, Circuit Description

This discourse is based on the following schematic sets: the GN Modulator printed circuit assembly, the Data_FPGA, and the Mod_FPGA. Most of the digital logic is contained within the two Xilinx Spartan FPGAs, making it necessary to have all three schematic sets on hand when tracing the signal flow. The text will use the following naming convention; PCB is shorthand for the printed circuit assembly schematic set, DATA is shorthand for the Data_FPGA schematic set, and MOD is shorthand for the Mod_FPGA schematic set.

PCB Sheet One is a simple block diagram that connects the other PCB schematic sheets. Each block represents a schematic sheet and the page number is located at the top of each block. Signals on the left side of a block are inputs or bi-directional and signals on the right side of a block are outputs or bi-directional. The signals are grouped to make it easier to locate them on another block. Input signals that are tightly grouped will have a matching output group on another block. Input signals that are loosely grouped come from an output group on another block, but the spaces indicate that they do not use the entire group. This signal grouping convention does not apply to the FPGA schematic sets.

In reading this circuit description, the reader is encouraged to refer to the GMOD schematic diagrams (WSC-1547559), the two FPGA schematic sets (WSC-1547560 and WSC-1547561), and to the functional block diagram provided in Figure 3−1.

7−1   VMEbus Interface

PCB Sheet Two contains the portion of the VMEbus interface circuitry that is external to the FPGAs. The P1 connector is for the VMEbus backplane. The P2 connector provides the 50 MHz ECL clock, the User Clock and Data, the Bus Address Space select lines (BAS23..19), and the analog power connections. The GMOD card is installed in MDP Slot 5, and those BAS pins are hard wired on the backplane for address space

FC380000 − FC3FFFFF. When the VMEbus address bits and the address modifier bits are within the GMOD card address range, the Card Select Address Decoder (DATA, sheet 2) generates the Bd_Sel signal. That enables the interface hand-shaking circuitry, and a VMEbus data strobe will latch the address, enable the data transceivers, and start the strobe sequencer. The sequencer is a shift register that provides a sequence of strobes based on the 16 MHz VMEbus clock. The decoded address enables the appropriate registers and/or buffers for data transfer. A write operation generates a WrtStb that starts on Stb1 and ends on Stb2. A data_transfer_acknowledge signal (DTACK) is returned to the VMEbus when the sequencer generates Stb2. After the VMEbus controller inactivates the DSTB lines, the GMOD Stb lines are cleared and the bus interface returns to the "waiting" state. Note that VMEbus interrupter circuitry is not implemented in the Data_FPGA but provisions for such an enhancement are provided in the external glue logic (PCB, sheet 2).

The addressable VMEbus register set for the Data_FPGA is documented in Appendix A. The Data_FPGA control registers can be read back over the VMEbus to verify their contents. The FPGA_ID register and the DataStat register do not have control registers and are read-only. The Data_FPGA is assigned address space FC380000−FC3BFFFF, but most of these are unused. Reading a Data_FPGA address that is outside the defined register set will return a value of all ones (FFFF). The defined register set is contiguous, beginning with address FC380000 and ending with address FC380010. The BdRst register is used to reset all of the GMOD functions, while the FifoRst register clears only the Fifo contents. The DataCntl register controls the data flow functions and the DataStat register provides Data Fifo status. The Fmt register selects the differential encoding format. The Format command is binary encoded, but the 8-state decoding is performed automatically by the differential encoder Mux controls (DATA, sheet 4). The ClkDiv register sets the Subcarrier_Clock to Data_Clock

ratio for subcarrier and idle pattern modes (DATA, sheet 1). The ClkGap register provides a programmable means of setting a threshold level for declaring No_Clk_In. The FPGA_ID register contains the revision level of the FPGA configuration code. The high-byte is the major revision level and the low-byte is the minor revision level. The GMOD project delivered revision level 0101H. The Analog register provides control information for the 8.5 MHz IF filter selection, the 70 MHz input selector, and the 8.5 MHz test selector (PCB, sheet 7). The FilterSel and InputSel values are binary decoded on DATA Sheet Two before going to the Analog section. The VMEtest register provides a means of testing the VMEbus interface without changing any existing settings.

A portion of the Mod_FPGA VMEbus interface is contained in the Data_FPGA. This saves space in the Mod_FPGA while still allowing autonomous VMEbus register operation. This design philosophy allows a modification to be performed on one FPGA VMEbus register set without requiring changes to the other FPGA. Address bit LA18 is used to enable the circuitry associated with Mod_FPGA Read and Write operations. Some of the bus buffers and registers may appear redundant, but the extra levels are caused by differences in the CLB and IOB logic sections of the Xilinx Spartan FPGA.

7—2   P3 Test Connector

The P3 connector contains numerous test points along with the JTAG programming signals (PCB, sheet 2, schematic grid location "3"). Because the JTAG programming capability does not change the serial EEPROM contents, it provides a non-destructive way of testing FPGA design changes. It can also be used to redefine test points, but the reader should keep in mind that the Xilinx Place and Route software may decide to reroute signals because of changes, thereby altering signal timing. A VMEbus SYSRST signal will clear all setups on the GMOD card and will actually reload the FPGA configuration code. The jumper between JP4 pins 1 and 2 may be pulled to deactivate this FPGA reload, but it should always be installed before using the card in the WSC system. JP4 pins 3 and 4 are normally open.

Appendix C is a schematic for a Test Box that was constructed and used during the design verification testing. It was connected to the P3 connector using 50-pin ground plane ribbon cable.

7—3   Baseband Processing, Data FPGA and FIFO

PCB Sheet Three shows the Data_FPGA along with its connection to the serial EEPROM and the Data Fifo. Note that the Fifo IC contains two independent Fifo circuits and that either one can be selected for use via the VMEbus or jumpers at JP1. JP2 and the Mux provide a means of programming the Serial EEPROM in-circuit using a keyed ribbon cable and external Atmel Configurator interface. With no cable attached, normal EEPROM signal flow is selected via the pullup on D_SER_EN. The FPGA configuration process begins when the PGM_Neg line is pulled low by a VMEbus system reset. The FPGA will clear its configuration memory (continuously) while PGM_Neg is low. When the reset operation is complete, the FPGA INIT line transitions from low to high, and the FPGA program cycle commences (Master Serial mode = Mode pin tied low). CCLK from the FPGA will begin clocking data out of the EEPROM and into the FPGA. The DONE line goes high when the program cycle is complete. The FPGA then performs an internal startup sequence that initializes it for operation.

7—3.1 Data FIFO and FIFO Control

The Data Fifo signal flow is controlled by the FPGA circuitry on DATA Sheet Three. Subcarrier modulation requires that the data rate be a sub-multiple of the subcarrier rate and synchronous to it. Since the incoming user clock is asynchronous to the GMOD board Subcarrier clock, a data clock (DivClk) is developed that will allow the required synchronization. The Subcarrier clock divider circuitry is shown on DATA Sheet One. The ExtClk and the DivClk will likely drift in relation to each other, and this will cause bit slips unless an elastic-buffer is provided. A 256-bit Fifo is used on the GMOD to allow for $+/-$ 128 bit slips during any contiguous data stream.

The incoming clock and data inputs, located on DATA Sheet Three at grid location "5", can be

inverted via program control. A clock detector circuit (bottom of DATA, sheet 3) provides the ability to program how many consecutive missed clocks occur before declaring No_Clk_In. Normal operation of this circuit requires that the ExtClkIn and the DivClk be roughly equal in frequency. If, due to a mis-programmed DivClk ratio, the ExtClkIn rate is significantly less than the DivClk rate (20%), then the clock detector will not operate. This is not a problem during normal operation because the MDP firmware will program the proper rate. However, when using the MDP Memory Editor function to setup offline tests, this situation may arise. The Empty and Full flag circuitry is located above the clock detector at schematic grid level "B". It contains latches to capture an error event, but also provides an OR of the current flag status for checking Fifo initialization.

Next is the Data Fifo reset circuitry located at about the middle of the page. The 16 MHz VMEbus SysClk is used to reset the Fifo by generating eight simultaneous Fifo_Write_Clk and Fifo_Read_Clk pulses while the Fifo_Reset line is held low. Additional pulses are then sent after the Fifo_Reset line goes high to initialize the Fifo flags. Completion of the reset cycle clears the FifoRst control register on DATA Sheet Two, reselecting ExtClk as the Fifo_Write_Clk and DivClk as the Fifo_Read_Clk.

The data paths are located above the reset circuitry at about the "C" grid level on the schematic. Switching is provided for selecting either "direct" ExtData or "elastic-buffered" Fifo-Data as input to the differential encoder circuit. When set for FifoData, the source can be either the actual Fifo Read Data or the Idle Pattern toggle flip-flop.

The top portion of DATA Sheet Three contains the Fifo Read Enable circuitry. When the Fifo_Ena line is active, the incoming data stream (ExtDataIn) is written to the Fifo using the associated input clock (ExtClkIn). When the Fifo is half full, FifoRdEna becomes active and the FIFO_Read_Clk begins clocking out the Read_Data. If the input clock stops (No_Clk_In), then the Fifo read continues until the Empty condition occurs and resets the ReadEna line. If the input stream stops before the

Fifo is half full, then the No-Clk_In condition will start the read process and empty the Fifo. This same mechanism is used for direct modulation with idle pattern enabled. Whenever the Fifo empties, the idle pattern becomes the input to the differential encoder circuit. The Fifo is necessary for this mode because it buffers the start of the data stream so that nothing is lost during the clock detection and data switchover operation. It also means that, when switching between the user data and the idle pattern, there will be no "jerks" because both are clocked from the same source.

7−3.2 Differential Encoding

DATA Sheet Four is the differential encoder circuit. The eight possible configuration commands are shown in the table, but two are redundant, so there are only six configurations. Schematic grid locations "5" and "4" contain the NRZL Mark/Space Converter. NRZ-M is generated by XORing the input data with the latch output data. NRZ-S is generated by XORing the input data with the inverted latch output data. Schematic grid locations "3" and "2" contain the BiPhase Converter. BiPhase-L data is generated by XORing the NRZL data with the clock. This data is registered using a 2X clock generated by XORing the clock with a delayed clock. BiPhase-M data is generated by XORing the NRZ-S data with the clock, and BiPhase-S data is generated by XORing the NRZ-M data with the clock.

7−4 Waveform Synthesis, Modulator FPGA and Support ICs

The Mod_FPGA, in conjunction with the SRAM found on PCB Sheets Five and Six, synthesizes the desired IF waveform. It also controls the process of initializing all SRAM with values contained in the EPROMs. Mod_FPGA Sheet One shows four hierarchical blocks, a test point Mux, various output buffers, and the input buffer for the 15-bit subcarrier magnitude. One may notice an apparent inconsistency in that some input and output buffers are instantiated in the schematic, while others are not. I/O buffers are instantiated in the schematic for two reasons: 1) to ensure a latching function occurs in the I/O block circuitry, and 2) to route the same signal to more than one device pin (with different names).

7−4.1 Mod_FPGA Programming

PCB Sheet Four shows the Mod_FPGA along with its connection to the serial EEPROM. JP3 and the Mux provide a means of programming the Serial EEPROM in-circuit using a keyed ribbon cable and external interface. With no cable attached, normal EEPROM signal flow is selected via the pullup on D_SER_EN. The FPGA configuration process begins when the PGM_Neg line is pulled low by a VMEbus system reset. The FPGA will clear its configuration memory (continuously) while PGM_Neg is low. When the reset operation is complete, the FPGA INIT line transitions from low to high, and the FPGA program cycle commences (Master Serial mode = Mode pin tied low). CCLK from the FPGA will begin clocking data out of the EEPROM and into the FPGA. The DONE line goes high when the program cycle is complete. The FPGA then performs an internal startup sequence that initializes it for operation.

7−4.2 Mod_FPGA VMEbus Interface

The addressable VMEbus register set for the Mod_FPGA is documented in Appendix B. Mod_FPGA Sheet Two is the VMEbus interface circuit for the Mod_FPGA control and status registers and corresponds to the "VMEbusIntrfc" block of Sheet One. The addressable VMEbus register set for the Mod_FPGA is documented in Appendix B. The Mod_FPGA is assigned address space FC3C0000−FC3CFFFF, but most of these are unused. Reading a Mod_FPGA address that is outside the defined register set will return a value of all ones (FFFF). The defined register set is contiguous, beginning with address FC3C0000 and ending with address FC3C0014. Most of the Mod_FPGA control registers are not "read-what-you-write" registers, as is the case with the Data_FPGA registers. Each register in this address range configures or controls a different function; reading any register in this address range will return the same 16-bit status, the contents of the Configuration Status Register." This status register contains the aggregate status of all configurations controlled by writing to registers FC3C0000 − FC3C0014. The "Subcarrier Firmware Control Registers," FC3C0010 and FC3C0012, are true read/write registers. The

FPGA_ID register, FC3C0014, is a read-only register and, following the same convention as the ID register of the Data_FPGA, identifies the FPGA programming revision.

Setting bit zero of the "Run Register" will enable all modulation functions to operate; clearing this bit will disable all modulation functions, as will setting bit zero of the "Mod Reset" register. The value of bit zero of the "Configuration/Status Register" reflects the run status of the Mod_FPGA.

Setting bit zero of the "SRAM Load Register" will commence the process of loading all SRAM with EPROM contents. Clearing this bit has no affect on the SRAM load process. The value of bit two of the "Configuration/Status Register" reflects current status of the SRAM load process.

Setting bit zero of the "Carrier Mod Enable" Register configures the modulator to enable carrier modulation; clearing this bit will configure the Mod_FPGA to synthesize a CW signal. Bit three of the "Configuration/Status Register" reflects the current contents of this register.

Setting bit zero of the "Data Mod Enable" Register configures the modulator to enable data modulation; clearing this bit will configure the Mod_FPGA to disable data modulation. (For direct PM configurations, this would have the same effect as the "carrier modulation enable configuration." For subcarrier configurations, this allows for disabling data modulation of the subcarrier without disabling subcarrier modulation of the carrier.) Bit four of the "Configuration/Status Register" reflects the current contents of this register.

Bits 1−0 of the "Modulation Configuration Register" configure the Mod_FPGA for different modulation formats. Bits 6−5 of the "Configuration/Status Register" reflect the current contents of this register.

Bits 3−0 of the "Modulation Index Register" are used to select the desired modulation index for all modulation configurations. Bits 12−8 of the "Configuration/Status Register" reflect the current contents of this register.

Bits 2−0 of the "Test Point Select Register" configure the Test Point Mux (Mod_FPGA Sheet One) to select the desired data to be routed to the

Mod_FPGA test point pins 15−0. Bits 15−13 of the "Configuration/Status Register" reflect the current contents of this register.

Setting bit zero of the "Mod Reset Register" will reset the Mod_FPGA. This will disable all modulation functions and will force the "Carrier Modulation" and "Data Modulation" configurations to the default disabled state. The value of bit one of the "Configuration/Status Register" reflects the current state of the reset process; a one indicates that a reset is in progress, while a zero indicates no reset is in progress (reset has completed).

The "Subcarrier Firmware Control Registers" configure the subcarrier frequency. Reading these registers will return the values contained in them.

7−4.3 Mod_FPGA Auto Leader

The Auto Loader circuit (Mod_FPGA Sheets 11−15) controls the process of loading the Carrier and Subcarrier SRAM with the contents of the Carrier and Subcarrier EPROM (PCB Sheets Five and Six). This process requires manipulation of the following signals and signal groups which are driven by the Mod_FPGA (refer to Mod_FPGA Sheet One and PCB Sheet 4−6): the EPROM address bus (EpromBus[18..0]), the Carrier and Subcarrier Address Buses (SramBusCar[17..0] and SramBusSub[17..0]), the EPROM and SRAM Chip Select signals (EpromCSN[2..0], SramCSN[5..0], and CarrierSramCSN), the SRAM Write Enable signal (Sram_wen), and the EPROM and SRAM Output Enable signals (EpromOEN and SramOEN). The Mod_FPGA also controls the SRAM Upper and Lower Byte Select signals (Sram_ub and Sram_UBN and Sram_LBN); however, these signals are "hard wired" to the enable state within the Mod_FPGA.

Mod_FPGA Sheet Eleven also contains the multiplexer function which determines which circuit is driving the SRAM address signals, the Auto Loader circuit during the SRAM Load process, or the Modulator and Subcarrier circuits when the Mod_FPGA is placed in Run mode.

This Auto Load process involves enabling all EPROM outputs and disabling all SRAM outputs, incrementing the Address lines driving the EPROMs and SRAMs, and generating a write pulse to latch the EPROM data into the SRAM for each address value. The single carrier SRAM IC is loaded with one sinewave image of 65,536 14-bit samples. The entire subcarrier SRAM space spans six SRAM ICs. This space is loaded with nineteen ¼-sinewave images, each of 65,536 15-bit samples. Each image is scaled for the modulation index for which it is selected. (One 65,536-point, 15-bit, ¼-sinewave image is used to construct a 262,144-point, 16-bit, full-sinewave image by the Subcarrier Generation circuit.)

Block V1 of Mod_FPGA Sheet 11 (Grid Location D5) divides the 50 MHz sample clock by sixteen to generate divclk, a 3.125 MHz clock; this is the clock rate at which the SRAM is loaded. V1 also generates one Write Pulse during each period of the divided clock (wen_pulse); this signal is used to latch the data into the SRAM. V1 is implemented as VHDL code (Mod_FPGA Sheet 14).

Block V2 of Mod_FPGA Sheet 11 (Grid Location D4) provides the address increment function; it is also implemented as VHDL code (Mod_FPGA Sheet 15). This module is implemented as a state machine which is driven by the 3.125 MHz clock. When SRAMLoad goes high (as a result of the VMEbus SRAM Load control bit being set) the state machine enters the Increment State and, starting at a value of zero, increments the address lines on each successive clock period. When all SRAM ICs have been loaded, the state machine enters its "wait state," remaining there until it receives another SRAMLoad pulse.

The EPROM Chip Select signals are manipulated to enable the EPROM chips successively as the load process proceeds through the entire address space, as determined by the upper address count bits (Mod_FPGA Sheet 11, Grid Location B3). The Carrier SRAM Chip Select signals are manipulated in a similar manner during the load process, and are determined by the upper three bits of the configured Modulation Index when in run mode (Mod_FPGA Sheet 11, Grid Location A3).

The EPROM Address Bus signals are driven by the incrementing address counter (ABUS[20..0]) during the load process (Mod_FPGA Sheet 11, Grid Location B3). (The P2 Block in this circuit is a pass through which is utilized to work around the

OrCAD limitation that a signal cannot have multiple aliases; see Mod_FPGA Sheet 13.) When in run mode, the EPROM outputs are disabled.

The SRAM Address Buses are driven by the incrementing address counter (ABUS[20..0]) during the load process. When in the run mode, the Carrier SRAM Address Bus is driven by a Carrier phase bus which is generated by the Modulator circuit. When in the run mode, the two most significant bits of the Subcarrier SRAM Address Bus are driven by the two least significant bits of the configured Modulation Index (Mod_FPGA Sheet 11, Grid Location A3—B4). The remaining address bits are driven by the Subcarrier phase bus, which is generated by the Subcarrier generation circuit.

7—4.4 Carrier Modulation

PCB Sheet Seven shows the GMOD IF circuit. This analog circuit is driven by the analog output of the DAC (Grid Location D5). The inputs of the DAC are driven by the carrier SRAM. Prior to being placed in Run mode, the Mod_FPGA must load this SRAM with the digital sinewave image contained in the carrier EPROMs (PCB Sheet Six). To generate the desired signal, the Address bus of the SRAM must represent the changing phase of the signal. This phase signal is generated by the Modulator circuit, Mod_FPGA Sheet Six.

A 32-bit adder is configured as a 32-bit accumulator (Mod_FPGA Sheet Six, Grid Location A4) by connecting its output to one of the inputs. Its other input determines the step increase for each sample clock period. This input is driven by the constant 730,144,440, generating the component at Grid Location A5. With a 32-bit accumulator and a sample rate of 50 MHz, this phase step increase generates the desired 8.5 MHz carrier. Driving the Address bus of the Carrier SRAM directly with this accumulator output would step through sinewave image in equal increments, producing a CW signal. (This is essentially the configuration achieved when the modulator is configured for carrier modulation disabled.) The output of the 32-bit adder used for this function is a 33-bit value. Because the phase calculation is a modulo-32

arithmetic process, this "carry bit" is not used in this application.

The output of the Carrier Accumulator is presented to a 16-bit adder (Mod_FPGA Sheet 6, Grid Location A2—B2). Adding a value to the accumulator output is equivalent to adding a phase offset to the sinewave signal. The phase input of this adder is selected from one of three signals by the three-to-one, "Phase Selector" multiplexer (Mod_FPGA Sheet 6, Grid Location C2).

One of these signals is a constant zero, selected when carrier modulation is disabled.

The B-input of the Phase Selector is the digital, BPSK-modulated subcarrier, generated by the 16-bit inverter labeled "BPSK Modulator" (Mod_FPGA Sheet 6, Grid Location B4). This inverter performs a 1's complement inversion on the 16-bit subcarrier based on the sense of the data, as sampled by the latch at Grid Location C5. The data is latched by the most significant bit of the subcarrier, the subcarrier clock. This ensures that data transitions, as applied to the subcarrier modulation, are coincident with subcarrier zero-crossings.

The A-input of the Phase Selector is the output of the two-to-one selector at Grid Location D3. The two inputs to this selector are driven by the contents of the two Look-up-Tables at Grid Location D5. The value selected from each table is determined by the configured modulation index. Any two values corresponding to the same modulation index represent positive and negative phase offsets of equal-magnitude. The values of these Look-up-Tables are found in Table 7—1. (Note that because the carrier phase processing is performed in unsigned modulo arithmetic, a negative phase is effected by a positive phase representing an angle that is 2π radians minus the modulation index.) Location-zero, selected when the modulation index register is programmed to zero, contains values that correspond to a mod index of $\pi/2$. This configuration will produce BPSK modulation when the modulator is configured for direct carrier PM. When the modulator is configured for squarewave subcarrier modulation, this will result in a completely suppressed carrier.

The Phase Offset selected by the selector at Grid Location D3 is one of two values. For Direct PM

		Positive Phase		Negative Phase	
Table Offset	Mod Index	Decimal	Hex	Decimal	Hex
0	π/2	16,384	4000	49,152	C000
1	0.1	1,043	413	64,493	FBED
2	0.2	2,086	826	63,450	F7DA
3	0.3	3,129	C39	62,407	F3C7
4	0.4	4,172	104C	61,364	EFB4
5	0.5	5,215	145F	60,321	EBA1
6	0.6	6,258	1872	59,278	E78E
7	0.7	7,301	1C85	58,235	E37B
8	0.8	8,344	2098	57,192	DF68
9	0.9	9,387	24AB	56,149	DB55
10	1.0	10,430	28BE	55,106	D742
11	1.1	11,473	2CD1	54,063	D32F
12	1.2	12,516	30E4	53,020	CF1C
13	1.3	13,559	34F7	51,977	CB09
14	1.4	14,603	390B	50,933	C6F5
15	1.5	15,646	3D1E	49,890	C2E2
16	1.6	16,689	4131	48,847	BECF
17	1.7	17,732	4544	47,804	BABC
18	1.8	18,775	4957	46,761	B6A9

Table 7−1. Phase Offset Lookup Tables

Modulation, the positive or negative phase offset is selected based on the sense of the data. For Squarewave Subcarrier Modulation, the selection is made based on the sense of the modulated squarewave subcarrier. This squarewave subcarrier is generated by the XOR gate at Grid Location C4, and is the product of the exclusive-OR operation of the subcarrier clock (squarewave subcarrier) and the data.

7−4.5 Subcarrier Generation

The subcarrier is constructed from a ¼-sinewave stored in the subcarrier SRAM. This full-sinewave construction is performed by the circuit shown on Mod_FPGA Sheet Nine. As with the carrier phase generation, the subcarrier phase generation begins with a 32-bit adder that is wired as a 32-bit accumulator (Grid Location C3−D4). The B-input

to this accumulator (the phase step size) is configured by the Subcarrier Firmware Control Word registers via the VMEbus interface. This value determines the frequency of the subcarrier.

The ¼-sinewave image stored in SRAM represents the first quadrant of a sinewave. These values are used as the magnitude values for all four quadrants of the constructed sinewave. Address bits 31 and 32 determine the quadrant that is currently being constructed, and are used to control the processing appropriate to the current quadrant. Address bits 14−29 of the accumulator are used to generate the Subcarrier SRAM address bus. This accumulator value must be inverted for quadrants two and four, as is accomplished by the 16-bit, 1's complement inverter at Grid Location C2. Consequently, for quadrants one and three, the values are read from low address to high address, corresponding to a positive phase rotation of zero to $\pi/2$, while in quadrants two and four the values are read from high address to low address, corresponding to a negative phase rotation of $\pi/2$ to zero. Thus, the sequence of values read from the subcarrier SRAM represent a 15-bit, rectified sinewave (SubCarMag[14..0], Grid Location C5).

To complete the generation of the full-sinewave subcarrier, these magnitude values must be inverted for quadrants three and four. This is achieved by the SubCarGeneration Block at Grid Location B3−B2, whose circuit is shown on Sheet 10. This process involves performing a 1's complement inversion on the 15-bit amplitude

data for quadrants three and four, and appending the 1's complement sign bit as the most significant bit for all quadrants, generating the 16-bit, 1's complement, full-sinewave subcarrier.

7−4.6 Mod_FPGA Test Points

Twenty Mod_FPGA pins are designated as test points and are routed to the P3 connector (PCB Sheet Two), where they are labeled Mod_TP0 through Mod_TP19. Of primary interest are Mod_TP0 through Mod_TP15. Via the Test Point Select register of the VMEbus interface, any one of six, 16-bit, internal databuses can be presented to these test points. The available signals are listed in Table 7−2.

7−5 Analog Conversion and IF Processing

7−5.1 DAC Implementation

The IF Section (PCB, sheet 7) is where the Digital data becomes an Analog signal. The Carrier SRAM data is latched into the DAC by the 50 MHz clock. The digital side of the DAC is powered by a small 3.3V regulator to ensure TTL signal level compatibility. The regulator power source is the VCC_AN, so the relatively quiet Analog voltage plane powers both sides of the DAC. A ferrite bead connects the Analog and Digital ground planes and prevents any large potential differences from building up when the board is out of the system.

Table 7−2. Test Point Selection		
Test Point Select	Modulator FPGA Signals	Description
0	SubCarPhase	The 16 MSB of the Subcarrier SRAM Address bus
1	CarAccum	The 16 MSB of the output of the Carrier Accumulator
2	PMPhase	The 16-bit phase to be added to the Carrier Accumulator value
3	SubCar	The full-sinewave Subcarrier as generated by the FPGA
4	BPSKSubCar	The Subcarrier after being BPSK modulated by the data
5	CarPhase	The 16 MSB of the Carrier SRAM Address bus

The FS_ADJ potentiometer is wired as a rheostat and it should be set at 2k ohms to get the full-scale output of the DAC.

7−5.2 IF Processing

The 8.5 Mhz analog output is low-pass filtered and transformer coupled to a GaAs switch. Control of the various IF Section switches is via the "Analog" VMEbus register in the Data_FPGA. The analog chain can be tested separately from the digital circuitry by injecting a signal into the 8.5 MHz Test IF front panel SMB connector (J1). All of the levels shown on the schematic are approximations and will vary from board to board. A pair of GaAs switches controls the 8.5 MHz IF filter bank. Due to economic considerations and projected user requirements, only the 256 kHz BW and the 4 MHz BW filters are installed on the final product. The pads at the filter outputs are used to roughly match the levels so that switching filters does not drastically change the mixer IF input level. The 8.5 MHz IF is mixed with the 61.5 MHz LO (J3) coming from the SYNTH board. The resulting 70 MHz output is passed through a 4 MHZ BW filter, gain adjusted, and then fed to the 70 MHz Input Select switch. This switch selects between the GMOD, the FMOD (J5), or two auxiliary 70 MHz IF sources (J7, J8). The 70 MHz output of the GMOD card (J4) is returned to the FMOD card and is eventually upconverted to 370 MHz by the FMOD card. (The remaining front panel connectors, J2 and J6, are −20dB test points.)

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Appendix A. GMOD Data_FPGA VMEbus Addresses and Bit Functions

Register Name	ADDR	Type	Bit	Write Definition	Read Definition
Reset GMOD	FC380000	R/W	0	0 = No affect 1 = Reset all board functions	0 = Reset complete 1 = Reset in progress
Reset Fifo	FC380002	R/W	0	0= No Effect 1= Reset FIFO	0= FIFO Reset complete 1= FIFO Reset in progress

Data Control
    Run
 	
    FIFO Enable
 	
    Idle Enable
 	
    Data Invert
 	
    Clock Invert
 	
    FIFO Select Enable
 	
    FIFO Write Select
 	
    FIFO Read Select
 	
    Subcar Test Select
	FC380004	R/W	
			0
			
			1
			
			2
			
			3
			
			4
			
			5
			
			6
			
			7
			
			15
				
				0 = Halt
				1 = Run
				0 = Disable FIFO
				1 = Enable FIFO
				0 = Disable Idle Pattern Gen.
				1 = Enable Idle Pattern Gen.
				0 = No Data Inversion
				1 = Invert Input Data
				0 = No Clock Inversion
				1 = Invert Input Clock
				0 = Disable bit 6 & 7 Pgm Control
				1 = Enable bit 6 & 7 Pgm Control
				0 = Select FIFO 1 for write
				1 = Select FIFO 2 for write
				0 = Select FIFO 1 for read
				1 = Select FIFO 2 for read
				0 = Normal Subcarrier
				1 = Subcarrier from P3, pin 21
					Configuration Readback

Status
    FIFO Error
 	
    FIFO Empty
 	
    FIFO Full
 	
    FIFO Half Full
 	
    FIFO AF/AE
 	
    No Clock In
 	
    FIFO Write Select
 	
    FIFO Read Select
	FC380006	R	
			0
			
			1
			
			2
			
			3
			
			4
			
			5
			
			6
			
			7
				No Write Functions Supported	
					0 = No error
					1 = Illegal Full or Empty Event
					0 = FIFO is not empty
					1 = FIFO is Empty
					0 = FIFO is not Full
					1 = FIFO is Full
					0 = FIFO is not Half Full
					1 = FIFO is Half Full
					0 = FIFO is not AF/AE
					1 = FIFO is Almost Full / Empty
					0 = Input Clock present
					1 = Input Clock is not present
					0 = Write to FIFO1
					1 = Write to FIFO2
					0 = Read from FIFO1
					1 = Read from FIFO2

Format	FC380008	R/W	2−0	0 = NRZ−L (use 1) 1 = NRZ−L 2 = NRZ−M 3 = NRZ−S 4 = BIPHASE−L (use 5) 5 = BIPHASE−L 6 = BIPHASE−S 7 = BIPHASE−M	Configuration Readback
Subcarrier Clock Divide (ratio of Subcarrier Freq. to Data Rate)	FC38000A	R/W	2−0	0 = Divide by 1 1 = Divide by 2 2 = Divide by 4 3 = Divide by 8 4 = Divide by 16 5 = Divide by 32 6 = Divide by 64 7 = Divide by 128	Configuration Readback

Register Name	ADDR	Type	Bit	Write Definition	Read Definition
Clock Gap	FC38000C	R/W	7−0	Number of missed clock cycles to declare no clock present. Valid range is 2 to 64 (2 is nominal).	Configuration Readback
Rev Level	FC38000E	R	15−0	No Write Functions Supported	15−8 = Major revision level 7−0 = Minor revision level

Analog Control
  IF Filter Select
 	
  IF Input Select
 	
8.5 MHz Test IF
	FC380010	R/W	
			1−0
			
			3−2
			
			4
				
				0 = 256 kHz
				1 = 1 MHz
				2 = 2 MHz
				3 = 4 MHz
				0 = GMOD Modulation
				1 = FMOD Modulation
				2 = External Mod 1
				3 = External Mod 2
				0 = Select DAC Output
				1 = Select 8.5 MHz Test Input
					Configuration Readback

R/W Test Register	FC380012	R/W	15−0	16−bit register for VMEbus testing	Configuration Readback

[1] Installation of the "FIFO Manual Select" jumper(JP1, pins 5−6) on the PCB oversides any VMEbus programmed selection. When the PCB is jumpered for manual select, JP1 pins 1−2 unjumpered selects FIFO1 for Writes, jumpered selects FIFO2. JP1 pins 3−4 unjumpered selects FIFO1 for Reads, jumpered selects FIFO2.

Appendix B. GMOD Mod_FPGA VMEbus Addresses and Bit Functions

Register Name	ADDR	Type	Bit	Write Definition	Read Definition
Modulator Run	FC3C0000	W[1]	0	0 = Modulator Halt 1 = Modulator Run	See Modulator Config Status
Modulator Reset	FC3C0002	W[1]	0	0 = No affect 1 = Reset Modulator	See Modulator Config Status
SRAM Load	FC3C0004	W[1]	0	0 = No affect 1 = Initialize SRAM	See Modulator Config Status
Carrier Mod Enable	FC3C0006	W[1]	0	0 = Modulation Disable 1 = Modulation Enable	See Modulator Config Status
Data Mod Enable	FC3C0008	W[1]	0	0 = Modulation Disable 1 = Modulation Enable	See Modulator Config Status
Modulation Type	FC3C000A	W[1]	1−0	0 = Direct Modulation 1 = Squarewave Subcarrier 2 = Sinewave Subcarrier 3= Undefined	See Modulator Config Status
Modulation Index	FC3C000C	W[1]	4−0	0 = Supressed Carrier 1 to 18 = 0.1 to 1.8 radians 19 to 31 = Undefined	See Modulator Config Status
Mod Test Point Select	FC3C000E	W[1]	2−0	0 = Subcarrier Phase 1 = Carrier Accumulator 2 = PM Phase 3 = Subcarrier 4 = BPSK Subcarrier 5 to 7 = Undefined	See Modulator Config Status
GN Mod Config Status Modulator Run		R[1]	0		0 = Modulator halted 1 = Modulator running
Modulator Reset			1		0 = Reset complete 1 = Reset in progress
SRAM Load			2		0 = SRAM Load complete 1 = SRAM Load in progress
Carrier Mod Enable			3		0 = Carrier Modulation disabled 1 = Carrier Modulation enabled
Data Mod Enable			4		0 = Data Modulation disabled 1 = Data Modulation enabled
Mod Type			6−5		0 = Direct Modulation 1 = Squarewave Subcarrier 2 = Sinewave Subcarrier 3 = Undefined
Mod Index			12−8		0 = Suppressed Carrier 1 to 18 = 0.1 to 1.8 radians 19 t0 31 = Undefined
Test Point Select			15−13		0 = Subcarrier Phase 1 = Carrier Accumulator 2 = PM Phase 3 = Subcarrier 4 = BPSK Subcarrier 5 to 7 = Undefined
Subcarrier FCW, High	FC3C0010	R/W	15−0	Frequency Control Word, Upper	Configuration Readback
Subcarrier FCW, Low	FC3C0012	R/W	15−0	Frequency Control Word, Lower	Configuraiton Readback
Rev Level	FC3C0014	R	15−0	No Write Functions Supported	15−8 = Major revision level 7−0 = Minor revision level

[1] Addresses 0000, 0002, 0004, 0006, 0008, 000C, and 000E function as unique write registers, but a read of any of these registers will display the GN Mod Configuration Status word. This is a 16−bit word containing the aggregate configuration of registers 0000 throught 000E.

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Appendix C. Sample GMOD P3 Test Box
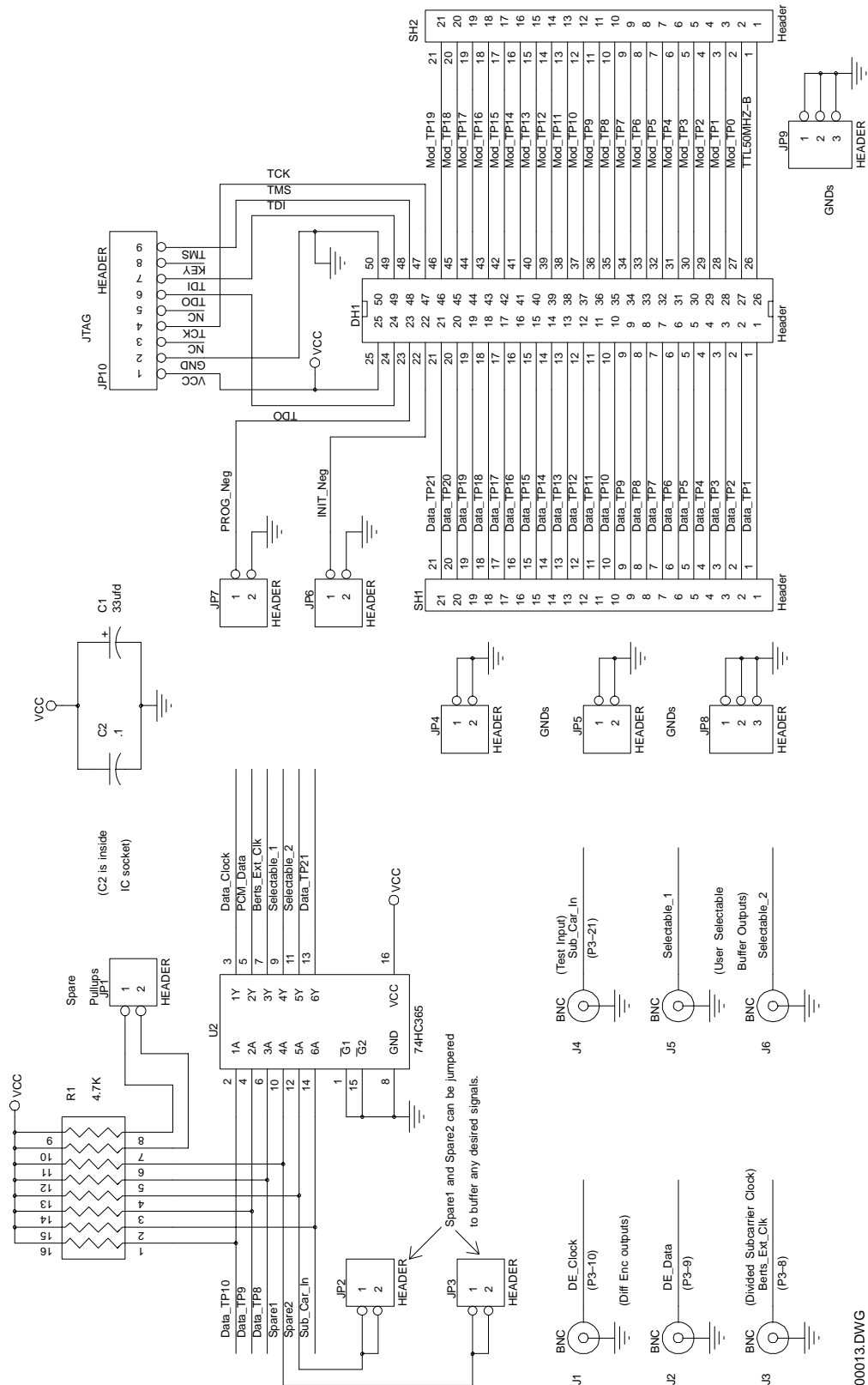
00013.DWG

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Glossary

The following defines the abbreviations, acronyms, and mnemonics used in this manual.

BPSK	Binary Phase Shift Keying		MHz	Mega—Hertz
CLB	Configuration Logic Block		NASA	National Aeronautics and Space Administration
DAC	Digital—to—Analog Converter		NRZ—L	Nonreturn to zero—level
DDS	Direct Digital Synthesis		NRZ—M	Nonreturn to zero—mark
DTACK	Data_Transfer_Acknowledge		NRZ—S	Nonreturn to zero—space
EEPROM	Electrically Erasable Programmable Read Only Memory		PCB	Printed Circuit Board
EPROM	Erasable Programmable Read Only Memory		PCM	Pulse Code Modulation
			PM	Phase Modulation
FIFO	First—in—First—Out		PSK	Phase Shift Keying
FPGA	Field Programmable Gate Array		PWA	Printed Wire Assembly
GMOD	Ground Network Modulator		QPSK	Quadrature PSK
GN	Ground Network		SN	Space Network
IF	Intermediate Frequency		SRAM	Static RAM
IOB	Input/Output Block		STGT	Second TDRSS Ground Terminal
LEO	Low Earth Orbiting		TDRSS	Tracking and Data Relay Satellite System
LO	Local Oscillator		TTL	Transistor—Transistor Logic
LRU	Line Replaceable Unit		VME	Versa—Moldule Europa
MCP	Modem Control Processor PWA		WSC	White Sands Complex
MDP	Modulator/Doppler Predictor			

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